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(54) Code generator for selectively producing cyclic redundancy check data codes different in data length

(57) A code generator incorporated in a transmitter has data paths (42d/41a to 41h/42a/43a/42b/43b; 42d/41a to 41p/42a/ 43a/ 42b/42c/43b) different in length for producing one of cyclic redundancy check codes (CRC8, CRC16) different in data length from a digital data signal (Din) supplied thereto, and circuit components of the data path shortest of all are shared with other data paths so that the code generator is fabricated from a small number of circuit components.

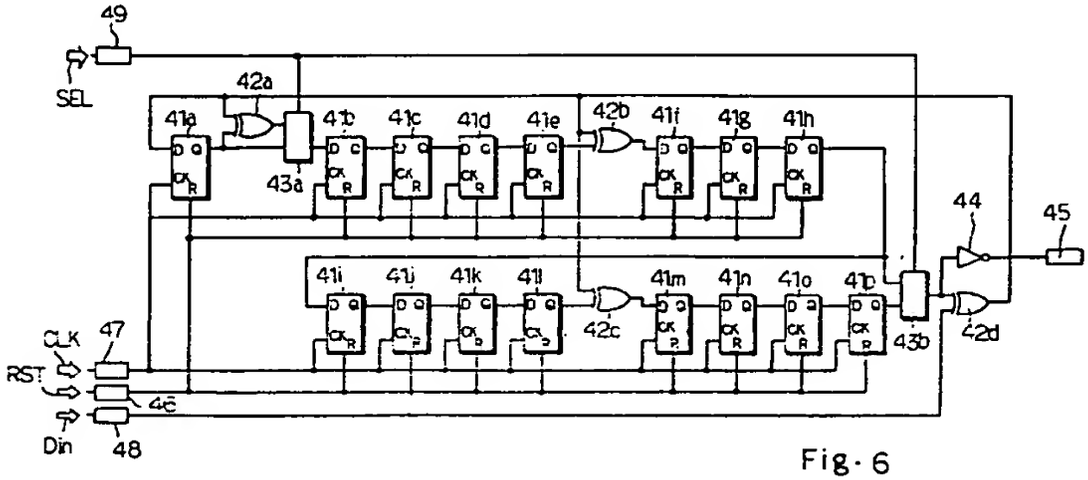

Fig. 6

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Description

FIELD OF THE INVENTION

This invention relates to a code generator for a cyclic redundancy check code and, more particularly, to a code generator for providing cyclic redundancy check codes different in data length to a transmission data frame.

DESCRIPTION OF THE RELATED ART

The cyclic redundancy check code is incorporated in a transmission data frame to see whether or not an error bit takes place in the transmission data code. Figures 1A and 1B illustrate two kinds of format of the transmission data frame. The first kind of format is illustrated in figure 1A, and the transmission data frame 1/2 has a transmission data field 1a/2a assigned to a transmission data code and a cyclic redundancy check data field 1b/2b assigned to a cyclic redundancy check code CRC. Although the transmission data frames 1/2 have different data length, they are coded into the same format. The transmission data field 1a is short, and is accompanied with an 8-bit cyclic redundancy check code CRC. On the other hand, the transmission data field 2a is long, and a 32-bit redundancy check code CRC is required. In the following description, the cyclic redundancy check code CRC is suffixed with the number of component bits. The 32-bit cyclic redundancy check code and the 8-bit cyclic redundancy check code are, by way of example, represented by "CRC32" and "CRC8", respectively.

The transmission data code is supplied to a code generator (see figures 2 and 3) incorporated in a transmitter, and the code generator produces the cyclic redundancy check code CRC8/CRC32 on the basis of the transmission data code. The cyclic redundancy check code CRC8/CRC32 is added to the transmission data code, and the transmission data code and the cyclic redundancy check code CRC8/CRC32 form in combination the transmission data frame 1/2. The transmitter sends the transmission data frame to a receiver (not shown).

A collator is incorporated in the receiver, and the transmission data frame 1/2 is supplied to the collator. The collator carries out a predetermined calculation to see whether or not the predetermined calculation results in expected value. If the calculation result is matched with the expected value, the collator decides the transmission data code not to contain any error. On the other hand, if the calculation result is inconsistent with the expected value, the collator decides that an error has been introduced into the transmission data code.

A transmission data frame 3 is differently formatted as shown in figure 1B. The transmission data frame 3 is used in a radio local area network defined in IEEE802.11. The transmission data frame 3 has a header field 3a assigned to a header and a data field 3b assigned to a transmission data code, and two cyclic redundancy check data fields 3c and 3d are added to the header field 3a and the data field 3b, respectively. The header is shorter than the transmission data code, and the cyclic redundancy check codes CRC16 and CRC32 are different in data length from each other. In this instance, the cyclic redundancy check code CRC16 consists of sixteen bits, and the cyclic redundancy check code CRC32 has thirty-two bits. The collator treats the transmission data frame 3 as similar to the above described transmission data frames 1/2.

Figure 2 illustrates the prior art code generator 10 available for the 8-bit cyclic redundancy check code. Eight flip flop circuits 11a, 11b, 11c, 11d, 11e, 11f, 11g and 11h, three exclusive-OR gates 12a, 12b and 12c and an inverter 13 form in combination the prior art code generator 10. The flip flop circuits 11a to 11h are connected in cascade, and the exclusive-OR gates 12a/12b/12c are associated with the flip flop circuits 11a/11e/11h. The output nodes Q of the flip flop circuits 11a/11e are respectively connected to the input nodes of the exclusive-OR gates 12a/12b, and the output nodes of the exclusive-OR gates 12a/12b are connected to the input nodes D of the next flip flop circuits 11b/11f. The output node Q of the last flip flop circuit 11h is connected to an input node of the exclusive-OR gate 12c, and the output node of the exclusive-OR gate 12c is connected to the input node D of the first flip flop circuit 11a. Thus, the flip flop circuits 11a to 11h and the exclusive-OR gates 12a to 12c form a data path, and the output node Q of the last flip flop circuit 11h is connected through the inverter 13 to a data output terminal 14.

The prior art code generator 10 has a reset terminal 15 connected to the reset nodes of the flip flop circuits 11a to 11h, a clock node 16 connected to the clock nodes of the flip flop circuits 11a to 11h and a data input node 17 connected to the other input node of the exclusive-OR gate 12c. The output node of the exclusive-OR gate 12c is further connected to the input nodes of the other exclusive-OR gates 12a/12b.

The flip flop circuits 11a, 11e and 11h are corresponding to terms X^8, X^5 and X, respectively, and the 8-bit cyclic redundancy check code $CRC8[G_8(X)]$ is given as follows.

$$G_8(X) = X^8 + X^5 + X + 1 \qquad \text{Equation 1}$$

On the other hand, the 16-bit cyclic redundancy check code is produced by a prior art code generator shown in figure 3. Eight flip flop circuits 11i to 11p are added to the data path, and the exclusive-OR gates 12a/12b/12c are asso-

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ciated with the flip flop circuits 11e/11l/11p, and the flip flop circuits 11e/11l/11p are corresponding to X^{16}, X^{12} and X^5, respectively. The 16-bit cyclic redundancy check code CRC16[$G_{16}(X)$] is given by equation 2.

$$G_{16}(X) = X^{16} + X^{12} + X^5 + 1 \quad \text{Equation 2}$$

Though not shown in the drawings, the 32-bit cyclic redundancy check code CRC32 is produced by a code generator. The code generator executes the calculation expressed by equation 3.

$$G_{32}(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1 \quad \text{Equation 3}$$

As described hereinbefore, the transmission data frame defined in IEEE802.11 has the cyclic redundancy check codes CRC16 and CRC32 different in data length, and the transmitter requires the code generators for the redundancy check codes CRC16 and CRC32. In the prior art transmitter, the code generators are connected in parallel to a multiplexer, and the header and the transmission data code are selectively supplied to the code generators.

Figures 4A and 4B illustrate the prior art transmitter. The prior art transmitter shown in figure 4A includes a first-in-first-out register FIFO, a parallel-to-serial converter 20 connected to the first-in-first-out register FIFO, the code generators 21/22 connected in parallel to the parallel-to-serial converter 20 and a multiplexer 23 connected in parallel to the parallel-to-serial converter 20 and the code generators 21/22. The data codes to be transmitted are firstly written into the first-in-first-out register FIFO, and enter into the waiting cue. The data codes are successively read out from the first-in-first-out register FIFO, and each data code is supplied to the parallel-to-serial converter 20. The parallel-to-serial converter 20 converts the data code to a serial data signal, and the serial data signal is supplied to the code generators 21/22 and the multiplexer 23. The multiplexer 23 transfers the serial data signal to an output terminal 24, and the serial data signal is stored in the header field 3a or the data field 3b. The code generators 21/22 produce the cyclic redundancy check codes CRC16/CRC32, and the multiplexer 23 selectively connects the code generators 21/22 to the output terminal 24 so as to store the cyclic redundancy check code CRC16/CRC32 to the appropriate cyclic redundancy check data field 3c or 3d.

If the prior art transmitter is used for the transmission data frames 1 and 2, the code generators 21/22 produces the cyclic redundancy check codes CRC8/CRC32 from the transmission data code 1a or 2a, and the multiplexer 23 selects one of the cyclic redundancy check codes CRC8 and CRC32. One of the code generators 21 and 22 may be activated depending upon the data length of the code.

The prior art transmitter shown in figure 4B also includes the first-in-first-out register FIFO, the parallel-to-serial converter 20, code generators 25/26 and a multiplexer 27. The code generators 25/26 produces the cyclic redundancy check codes CRC16/CRC32 from the serial data signal, and supply the cyclic redundancy check codes CRC16/CRC32 to the multiplexer 27 as a parallel data. The multiplexer 27 not only transfers the data code to the parallel-to-serial converter 20 but also selects one of the cyclic redundancy check codes CRC16/CRC32. The code generators 25/26 may be selectively activated after the transmission of the header and the transmission of the transmission data code.

In detail, each data code is supplied to the first-in-first-out register FIFO, and enters into a waiting cue. The first-in-first-out register FIFO successively supplies the data codes to the multiplexer 23. The multiplexer 23 transfers the data code to the parallel-to-serial converter 20, and the data code is converted to a serial data signal. The serial data signal is transferred to the output terminal 24 and the code generators 25/26. The serial data signal is delivered from the output terminal 24 as the header field or the data field. The code generators 25/26 produces the cyclic redundancy check codes CRC16/CRC32 from the serial data signal, and supply the cyclic redundancy check codes to the multiplexer 23 as the parallel data. The multiplexer 23 selects one of the cyclic redundancy check codes depending upon the kind of the data code, and transfers the cyclic redundancy check code CRC16 or CRC32 to the parallel-to-serial converter 20. The selected cyclic redundancy check code CRC16 or CRC32 is delivered from the output terminal 24 as either cyclic redundancy check data field 3c or 3d.

Figure 5 illustrates the data transmission through the prior art transmitter shown in figure 4A. The prior art transmitter is assumed to deliver the transmission data frame 3 to a receiver, and the code generators 21 and 22 produce the cyclic redundancy check code CRC16 and the cyclic redundancy check code CRC32 from the header and the transmission data code, respectively.

The reset signal for the code generator 21 is changed to the low level at time t1, and the parallel-to-serial converter 20 supplies the serial data signal representative of the header to the code generators 21/22 and the multiplexer 23 in synchronism with the clock signal. The code generator 21 starts the execution of the calculation expressed by equation 2 so as to produce the cyclic redundancy check code CRC16. However, the other code generator 22 still stands idle.

A controller (not shown) changes the control signal SEL1 to active level at time t2, and the control signal SEL1 is supplied to the multiplexer 23. The multiplexer 23 is responsive to the control signal SEL1 so as to transfer the serial data signal representative of the header to the output terminal 24. The header is supplied to the receiver as the header field 3a.

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The controller recovers the control signal SEL1 to inactive level at time t3, and changes the control signal SEL2 to the active level. The control signal SEL2 causes the multiplexer 23 to transfer the cyclic redundancy check code CRC16 from the code generator 21 to the output terminal 24. Then, the cyclic redundancy check code CRC16 is delivered to the receiver as the cyclic redundancy check data field 3c.

The reset signal for the code generator 22 is changed to the low level at time t4, and the code generator 22 becomes active. The parallel-to-serial converter 20 supplies the serial data signal representative of the transmission data code to the code generators 21/22 and the multiplexer 23. The code generator 22 starts the execution of the calculation expressed by equation 3 so as to produce the cyclic redundancy check code CRC32 from the serial data signal representative of the transmission data code. However, the reset signal for the code generator 21 is recovered to the high level at time t5, and the code generator 21 stops the calculation expressed by equation 2.

The controller changes the control signal SEL2 and the control signal SEL1 to the inactive level and the active level at time t5, respectively. The control signal SEL1 makes the multiplexer 23 transfer the serial data signal representative of the transmission data code to the output terminal 24, and the serial data signal representative of the transmission data code is delivered to the receiver as the data field 3b.

The controller changes the control signal SEL1 and the control signal SEL3 to the inactive level and the active level, respectively at time t6. Then, the multiplexer 23 provides a data path from the code generator 22 to the output terminal 24, and the cyclic redundancy check code CRC32 is delivered to the receiver as the cyclic redundancy check data field 3d.

The reset signal for the code generator 22 is recovered to the high level at time t7, and the controller changes the control signal SEL3 to the inactive level. Then, the prior art transmitter returns to the initial condition.

Thus, the prior art transmitter selectively distributes data codes different in data length to the code generators, and alternately delivers the cyclic redundancy check codes and the associated data codes. However, a problem is encountered in the prior art transmitter in a large number of the code generator as many as the cyclic redundancy check codes to be required. If the prior art transmitter is expected to produce two cyclic redundancy check data codes CRC8 and CRC16, eight flip flop circuits and three exclusive-OR gates are required for one of the code generators, and sixteen flip flop circuits and three exclusive-OR gates are required for the other of the code generators. As a results, the total number of flip flop circuits and the total number of the exclusive-OR gates are twenty-four and six, respectively. Thus, even if the prior art transmitter is expected to produce only two cyclic redundancy check codes, the large number of circuit components are required for the prior art code generating circuit, and the circuit configuration is complicated.

SUMMARY OF THE INVENTION

It is therefore an important object of the present invention to provide a code generator which selectively produces cyclic redundancy check codes different in data length.

To accomplish the object, the present invention proposes to change a data path depending upon a cyclic redundancy check code.

In accordance with one aspect of the present invention, there is provided a code generator supplied with a digital signal for selectively producing cyclic redundancy check codes respectively representative of cyclic redundancy check values through polynomials different in the maximum degree of a variable from one another, the code generator comprises a plurality of flip flop circuits equal in number to the maximum degree of the variable incorporated in the polynomials, and connected in cascade, exclusive-OR gate means selectively inserted into the cascade connection of the plurality of flip flop circuits and multiplexing means selectively inserted into the cascade connection, and the plurality of flip flop circuits, the exclusive-OR gate means and the multiplexing means form a plurality of data paths selectively used for calculating the cyclic redundancy check values.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the code generator will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which:

Figs. 1A and 1B are views showing the format for the transmission data frame;

Fig. 2 is a circuit diagram showing the circuit configuration of the prior art code generator for producing the 8-bit cyclic redundancy check code;

Fig. 3 is a circuit diagram showing the circuit configuration of the prior art code generator for producing the 16-bit cyclic redundancy check data code;

Figs. 4A and 4B are block diagrams showing the circuit configurations of the prior art transmitters for transmitting transmission data frames different from one another;

Fig. 5 is a timing chart showing the data transmission through the prior art transmitter shown in figure 4A;

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Fig. 6 is a circuit diagram showing the circuit configuration of a code generator according to the present invention;

Figs. 7A and 7B are block diagrams showing the circuit configurations of transmitters for transmitting different transmission data frames;

Fig. 8 is a timing chart showing a data transmission carried out by the transmitter; and

Fig. 9 is a circuit diagram showing the circuit configuration of another code generator according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

Referring to figure 6 of the drawings, a code generator embodying the present invention selectively produces an 8-bit cyclic redundancy check code CRC8 and a 16-bit cyclic redundancy check code CRC 16. The 8-bit cyclic redundancy check code CRC8 and the 16-bit cyclic redundancy check code represent cyclic redundancy check data values $G_8(X)$ and $G_{16}(X)$, and the cyclic redundancy check data values $G_8(X)$ and $G_{16}(X)$ are expressed by equations 1 and 2, respectively. Variable X in equation 1 has the maximum degree of 8, and variable X in equation 2 has the maximum degree of 16.

The code generator comprises sixteen flip flop circuits 41a, 41b, 41c, 41d, 41e, 41f, 41g, 41h, 41i, 41j, 41k, 41l, 41m, 41n, 41o and 41p equal to the maximum degree of variable X for the cyclic redundancy check code CRC16, four exclusive-OR gates 42a, 42b, 42c and 42d, two multiplexers 43a and 43b and an inverter 44. The flip flop circuits 41a to 41p, the exclusive-OR gates 42a to 42d and the multiplexers 43a and 43b are arranged in such a manner as to form a data path, and the eighth flip flop circuit 41h is further connected to the multiplexer 43b. The multiplexer 43b is connected through the inverter 44 to a data output terminal 45. A reset terminal 46 is connected to the reset nodes R of the flip flop circuits 41a to 41p, and a reset signal RST changes the output bits at the output nodes Q of all the flip flop circuits 41a to 41p to logic "1" level. The reset signal RST is supplied to the reset terminal 46 before the calculation for a cyclic redundancy check code CRC8/CRC16. A clock terminal 47 is connected to the clock nodes CK of the flip flop circuits 41a to 41p, and a serial data signal Din representative of a transmission data code or a header is supplied through the data input node 48 to the exclusive-OR gate 42d. A control signal SEL is supplied through a control terminal 49 to the multiplexers 43a and 43b, and changes the data path of the code generator as will be described hereinafter. The component bits of the serial data signal Din are rippled from the flip flop circuit to the next flip flop circuit in synchronism with a clock signal CLK, and the exclusive-OR gates 42a/42b/4c carry out the exclusive-OR operation between the output bit of the flip flop circuits 41a, 41e and 41h/41p and the output bit of the exclusive-OR gate 42d and a component bit of the serial data signal Din.

The number of the flip flop circuits 41a to 41p is equal to the maximum degree of variable X for the cyclic redundancy check code CRC16 longer than the other cyclic redundancy check code CRC8. In this instance, the 16-bit cyclic redundancy check code CRC16 is longer in data length than the 8-bit cyclic redundancy check code CRC8. The cyclic redundancy check data value $G_{16}(X)$ is expressed by equation 2, and the maximum degree of variable X is 16.

The number of the exclusive-OR gates 42a to 42d is equal to the number of terms X^n incorporated in the equations for the cyclic redundancy data codes CRC8/CRC16 where n is natural number, i.e., 1, 2, ... However, N1 does not contain the term $X^{n\text{-}max}$ with the maximum degree in the equation for the cyclic redundancy data code shorter in data length, and term $X^{n\text{-}com}$ common between the equations is counted as "1". In this instance, total number of terms X^n is six, i.e., X^8 ,X^5 ,X^1 ,X^{16} ,X^{12} and X5. The cyclic redundancy check code CRC8 is shorter in data length than the cyclic redundancy check code CRC16, and term $X^{n\text{-}max}$ is X^8 . Term X^5 is shared between the equations, and is counted "1". Terms X^8 and X^5 are deleted from the terms X^n . Then, the total number of terms X^n is decreased to four, and four exclusive-OR gates 42a to 42d are incorporated in the code generator. In this instance, degrees "n" are 1, 5, 12 and 16, and the exclusive-OR gates 42a to 42d are respectively inserted between the first flip flop circuit 41a and the second flip flop circuit 41b, between the fifth flip flop circuit 41e and the sixth flip flop circuit 41f, between the twelfth flip flop circuit 41l and the thirteenth flip flop circuit 41m and between the sixteenth flip flop circuit 41p and the first flip flop circuit 41a.

The number N2 of multiplexers 43a and 43b is equal to the number of term X^m incorporated in the equation for the cyclic redundancy check code shorter in data length where m is natural number 1, 2, ... However, if term $X^{m\text{-}com}$ is shared with the other equation, term $X^{m\text{-}com}$ is deleted from terms X^m. In this instance, equation 1 is used for the cyclic redundancy check code CRC8 shorter than the other code CRC16, and term X^5 is deleted from terms X^m . The total number of terms X^m is two in this instance, and degrees "m" are 1 and 8. For this reason, the multiplexers 43a and 43b are associated with the first flip flop circuit 41a and the eighth flip flop circuit 41h, respectively, and are connected between the exclusive-OR gate 42a and the second flip flop circuit 41b and between the eighth flip flop circuit 41h and the exclusive-OR gate 42d.

The multiplexer 43a selectively connects the output node Q of the first flip flop circuit 41a and the exclusive-OR gate 42a to the second flip flop circuit 41b, and the multiplexer 43b selectively connects the eighth flip flop circuit 41h and the

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sixteenth flip flop circuit 41p to the inverter 44. When the multiplexers 43a and 43b connect the exclusive-OR gate 42a and the eighth flip flop circuit 41h to the second flip flop circuit 41b and the inverter 44/exclusive-OR gate 42d, respectively, the code generator shown in figure 6 is equivalent to the code generator shown in figure 2, and produces the 8-bit cyclic redundancy check code CRC8. On the other hand, when the multiplexers 43a and 43b connect the first flip flop circuit 41a and the sixteenth flip flop circuit 41p to the second flip flop circuit 41b and the inverter 44/exclusive-OR gate 42d, the code generator shown in figure 6 is equivalent to the code generator shown in figure 3, and produces the 16-bit cyclic redundancy check code CRC16.

The equation for the cyclic redundancy check data value $G_8(X)$ has term X^1 . However, the equation for the cyclic redundancy check data value $G_{16}(X)$ does not have term X^1 . For this reason, the multiplexer 43a connects the exclusive-OR gate 42a to the second flip flop circuit 41b. Both equations have term X^5, and the exclusive-OR gate 42b is connected between the fifth flip flop circuit 11e and the sixth flip flop circuit 11f without a multiplexer. Although term X^{12} is only incorporated in the equation for the 16-bit cyclic redundancy check code CRC16, the exclusive-OR gate 42c is connected between the twelfth flip flop circuit 41l and the thirteenth flip flop circuit 41m without a multiplexer, because the 8-bit cyclic redundancy check code CRC8 is delivered from the eighth flip flop circuit 41h.

The code generator shown in figure 6 forms a part of a transmitter, and figures 7A and 7B illustrates two different circuit configurations. The transmitter shown in figure 7A includes a first-in-first-out register FIFO connected to a data source (not shown), a parallel-to-serial converter 51 connected to the first-in-first-out register FIFO, a code generator 52 connected to the parallel-to-serial converter 52, a multiplexer 53 connected between the parallel-to-serial converter 51/the code generator 52 and an output terminal 54 and a controller 55 for controlling the code generator 52 and the multiplexer 53. The code generator 52 is similar in circuit configuration to the code generator shown in figure 6.

The transmission data codes different in data length or the header code/transmission data code are supplied to the first-in-first-out register 51, and enter into a waiting cue. The transmission data codes or the header code/transmission code are sequentially read out from the first-in-first-out register FIFO, and the parallel-to-serial converter 51 produces the serial data signal Din from the read-out code.

The serial data signal Din is supplied to the code generator 52 and the multiplexer 53. The controller 55 supplies a control signal CTL of logic "1" level to the multiplexer 53, and causes the multiplexer 53 to transmit the serial data signal Din representative of the header or the transmission data code to the output terminal 54. The header code or the transmission data code is delivered to a receiver (not shown) as the transmission data field 1a/1b or the header field 3a.

The controller 55 resets the code generator 52, and changes the data path depending upon the read-out code with the control signal SEL. The code generator 52 accepts the serial data signal Din, and calculates the cyclic redundancy check value Gx(X) on the basis of the header code/transmission data code represented by the serial data signal Din. The controller 55 changes the control signal CTL to logic "0" level, and the multiplexer 53 transfers a serial data signal Dcrc representative of the cyclic redundancy check code CRCx to the output terminal 54. The serial data signal Dcrc is delivered to the receiver as the cyclic redundancy data field 1b/2b/3c/3d.

The transmitter shown in figure 7B includes the first-in-first-out register FIFO, a code generator 56 for producing a cyclic redundancy check code CRCx from the serial data signal Din, the parallel-to-serial converter 51, a multiplexer 57 connected between the first-in-first-out register/code generator FIFO/56 and the parallel-to-serial converter 51 and the controller 55. The code generator 56 supplies the cyclic redundancy check code CRCx to the multiplexer 57 as parallel data.

The transmission data codes 1a/2a or the header code/the transmission data code 3a/3b are accumulated in the first-in-first-out register FIFO, and, thereafter, are read out therefrom. The controller 55 causes the multiplexer 57 to connect the first-in-first-out register FIFO to the parallel-to-serial converter 51, and each read-out code is converted to the serial data signal Din. The serial data signal Din representative of the header code or the transmission data code is delivered to a receiver (not shown) as the header field 3a or the transmission data field 1a/2a/3b.

The controller 55 resets the code generator 56, and changes the data path to calculate the cyclic redundancy check value Gx(X) on the basis of the readout code. The serial data signal Din is accumulated in the code generator 56 in synchronism with the clock signal CLK, and carries out the calculation for the cyclic redundancy check value Gx(X).

The controller 55 causes the multiplexer 57 to connect the code generator 56 to the parallel-to-serial converter 51, and the code generator 56 supplies the cyclic redundancy check code CRCx through the multiplexer 57 to the parallel-to-serial converter 51. The parallel-to-serial converter 51 converts the cyclic redundancy check code CRCx to the serial data signal Din, and the serial data signal Din representative of the cyclic redundancy check code CRCx is delivered to the receiver as the cyclic redundancy check field 1b/2b/3c/3d.

Figure 8 illustrates the data transmission. The transmission data is assumed to be formatted as shown in figure 1B. However, the header code and the transmission data code are shorter than those of the prior art, and 8-bit cyclic redundancy data code CRC8 and 16-bit cyclic redundancy check code CRC16 are required for the header code and the transmission data code, respectively. The transmitter has the circuit configuration shown in figure 7A.

The controller 55 changes the reset signal RST to logic "0" level at time t11, and code generator 52 is changed to be ready for calculation. The controller 55 further changes the control signal CTL to logic "1" level, and the multiplexer

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53 provides a data path between the parallel-to-serial converter 51 and the output terminal 54. The controller 55 maintains the control signal SEL in logic "0" level, and the multiplexers 43a/43b select the exclusive-OR gate 42a and the eighth flip flop circuit 41h.

The header code is read out from the first-in-first-out register FIFO, and the parallel-to-serial converter 51 converts the header code to the serial data signal Din. The serial data signal Din is supplied to the multiplexer 53 and the code generator 52. The multiplexer 53 transfers the serial data signal Din to the output terminal 54, and the serial data signal Din representative of the header code is delivered to the receiver as the header field 3a.

On the other hand, the code generator 52 accumulates the serial data signal Din in synchronism with the clock signal CLK, and calculates the cyclic redundancy check value $G_8(X)$.

The controller 55 changes the control signal CTL to logic "0" level at time t12, and the multiplexer 53 connects the code generator 52 to the output terminal 54. Then, the serial data signal Dcrc representative of the cyclic redundancy check code CRC8 is supplied to the output terminal 54, and is delivered to the receiver as the cyclic redundancy check data field 3c.

Subsequently, the controller 55 changes the control signal SEL to logic "1" level at time t13, and the multiplexers 43a/43b select the first flip flop circuit 41a and the sixteenth flip flop circuit 41p. The code generator 52 is modified to calculate the cyclic redundancy check value $G_{16}(X)$. The controller 55 further changes the reset signal RST to logic "1" level, and the output nodes Q of all the flip flop circuits 41a to 41p are changed to logic "1" level. The controller 55 further changes the control signal CTL to logic "1" level, and the multiplexer 53 connects the parallel-to-serial converter 51 to the output terminal 54, again.

The transmission data code is read out from the first-in-first-out register FIFO, and the parallel-to-serial converter 51 converts the transmission data code to the serial data signal Din. The serial data signal Din representative of the transmission data code is transferred through the multiplexer 53 to the output terminal 54, and is delivered to the receiver as the transmission data field 3b.

The serial data signal Din is accumulated into the code generator 52 in synchronism with the clock signal CLK, and the code generator 52 calculates the cyclic redundancy check value $G_{16}(X)$.

The controller 55 changes the control signal CTL to logic "0" level at time t15, and the multiplexer 53 connects the code generator 52 to the output terminal 54, again. Then, the serial data signal Dcrc representative of the cyclic redundancy check code CRC16 is transferred through the multiplexer 53 to the output terminal 54, and is delivered to the receiver as the cyclic redundancy check data field 3d.

As will be appreciated from the foregoing description, the code generator according to the present invention changes the data path depending upon the data length, and the circuit components for a short cyclic redundancy check code is shared between the short data path and the long data path. This results in that a relatively small number of circuit components form a code generator producing cyclic redundancy check codes different in data length. The prior art transmitter requires twenty-four flip flops six exclusive-OR gates for the cyclic redundancy check codes CRC8 and CRC16. However, only 16 flip flop circuits and four exclusive-OR gates form the code generator shown in figure 6.

Second Embodiment

Turning to figure 9 of the drawings, another code generator embodying the present invention selectively produces a cyclic redundant check code CRC8 and a cyclic redundant check code CRC16. The sixteen-flip flop circuits 41a to 41p, the four exclusive-OR gates 42a to 42d, the two multiplexers 43a and 43b and the inverter 44 also form in combination the code generator implementing the second embodiment. The first difference between the first embodiment and the second embodiment is that the output node of the exclusive-OR gate 42a is directly connected to the second flip flop circuit 41b, and the second difference is that the multiplexer 43a is connected between the output node of the exclusive-OR gate 4d/a source of logic "0" level and the input node of the exclusive-OR gate 42a.

The multiplexer 43b selects the eighth flip flop circuit 41h in the presence of the control signal SEL of logic "0" level and the sixteenth flip flop circuit 41p in the presence of the control signal SEL of logic "1" level.

When the control signal SEL is changed to logic "0" level, the multiplexer 43a connects the output node of the exclusive-OR gate 42d to the input node of the exclusive-OR gate 42a. As a result, the code generator shown in figure 9 becomes equivalent to the prior art code generator shown in figure 2. On the other hand, the control signal SEL of logic "1" level causes the multiplexer 43a to connect the source of logic "0" level to the input node of the exclusive-OR gate 42a. In this situation, if the first flip flop circuit 41a outputs logic "0" level, the exclusive-OR gate 42a yields logic "0" level. On the other hand, if the output bit of the first flip flop circuit 41a is changed to logic "1" level, the exclusive-OR gate 42a yields logic "1" level. Thus, the output bit of the exclusive-OR gate 42a is identical in logic level with the output bit of the first flip flop circuit 41a, and the code generator shown in figure 9 becomes equivalent to the prior art code generator shown in figure 3.

The code generator shown in figure 9 achieves all the advantages of the code generator implementing the first embodiment, and is also available for the transmitter shown in figure 7A.

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Although particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the present invention.

For example, a code generator may produce any combination of cyclic redundancy check codes CRCx and CRCy such as, for example, CRC16 and CRC32.

Claims

1. A code generator supplied with a digital signal (Din) for selectively producing cyclic redundancy check codes (CRC8/CRC16) respectively representative of cyclic redundancy check values ($G_8(X)$/ $G_{16}(X)$) through polynomials (equations 1 and 2) different in the maximum degree of a variable (X) from one another, comprising:

   a plurality of flip flop circuits (41a to 41p) connected in cascade; and
   exclusive-OR gate means (42a to 42d) selectively inserted into the cascade connection of said plurality of flip flop circuits,
   characterized in that
   said plurality of flip flop circuits (41a to 41p) are equal in number to the maximum degree of said variable (X) incorporated in said polynomials, and in that
   said code generator further comprises multiplexing means (43a/43b) selectively inserted into said cascade connection, said plurality of flip flop circuits, said exclusive-OR gate means and said multiplexing means forming a plurality of data paths (42d/41a to 41h/43a/43b; 42d/41a to 41p/43a/43b) selectively used for calculating said cyclic redundancy check values.

2. The code generator as set forth in claim 1, in which a plurality of exclusive-OR gates (42a to 42d) serve as said exclusive-OR gate means, and are equal in number to terms (X^{16}, X^{12},X) of said variable (X) different in degree incorporated in said polynomials (equations 1 and 2) except for a term (X^8) with a maximum degree (8) smaller than other maximum degree or degrees (16) of said variable (X) respectively incorporated in other or others (equation 2) of said polynomials, terms (X^5) of said variable (X) equal in degree (5) being counted once, if any.

3. The code generator as set forth in claim 2, in which each of said terms (X^{16}, X^{12}, X) of said variable (X) different in degree and incorporated in said polynomials (equations 1 and 2) except for said term (X^8) with said maximum degree smaller than said other maximum degree or degrees of said variable respectively incorporated in said other or others of said polynomials is expressed as X^n where n is an arbitrary natural number (16, 12 or 1), and said digital signal (Din) is supplied through one (42d) of said plurality of exclusive-OR gates connected between one (41p) of said plurality of flip flop circuits serving as a final stage to another (41a) of said plurality of flip flop circuits serving as the first stage, the other or the others (42a to 42c) of said plurality of exclusive-OR gates being supplied with an output bit or output bits from other or others (41a, 41e, 41l) of said plurality of flip flop circuits each located at n-place from said first stage where n is said arbitrary natural number.

4. The code generator as set forth in claim 1, in which at least one multiplexer (43b) serves as said multiplexing means, and said at least one multiplexer has input nodes connected to certain flip flop circuits (41h/41p) selected from said plurality of flip flop circuits for serving as final stages of said plurality of data paths, said cyclic redundancy check codes (CRC8/CRC16) being supplied from said at least one multiplexer (43b).

5. The code generator as set forth in claim 1, in which said multiplexing means is implemented by a plurality of multiplexers (43a/43b) equal in number to terms (X^8, X) of said variable (X) of one (equation 1) of said polynomials having a term (X^8) with a maximum degree (8) smaller than other maximum degree or degrees (16) of said variable (X) respectively incorporated in other or others (equation 2) of said polynomials except for a term or terms (X^5) equal in degree (5) to other term or other terms (X^5) incorporated in said other or said others (equation 2) of said polynomials.

6. The code generator as set forth in claim 5, in which each of said terms (X^8, X) of said variable of said one of said polynomials having said term (X^8) with said smaller maximum degree (8) is expressed as X^m where m is an arbitrary natural number, and said plurality of multiplexers are respectively provided in association with certain flip flop circuits (41a/ 41h) selected from said plurality of flip flop circuits each located at m-place from one (41a) of said plurality of flip flop circuits serving as a first stage where m is said arbitrary natural number.

7. The code generator as set forth in claim 1, in which said exclusive-OR gate means is implemented by a plurality of

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exclusive-OR gates (42a to 42d) equal in number to terms (X^{16}, X^{12}, X^5, X) of said variable (X) different in degree and incorporated in said polynomials (equations 1 and 2) except for a term (X^8) with a maximum degree (8) smaller than other maximum degree or degrees (16) of said variable (X) respectively incorporated in other or others (equation 2) of said polynomials, terms (X^5) of said variable equal in degree being counted once, if any, and

said multiplexing means is implemented by a plurality of multiplexers (43a/43b) equal in number to terms (X^8, X) of said variable (X) of one (equation 1) of said polynomials having a term (X^8) with a maximum degree smaller than other maximum degree or degrees (16) respectively incorporated in other or others (equation 2) of said polynomials except for a term or terms equal (X^5) in degree to a term or terms (X^5) incorporated in said other or said others of said polynomials.

8. The code generator as set forth in claim 7, in which each of said terms (X^{16}, X^{12}, X^5, X) of said variable (X) different in degree except for said term (X^8) with the smaller maximum degree is expressed as X^n where n is an arbitrary natural number, and said digital signal (Din) is supplied through one (42d) of said plurality of exclusive-OR gates connected between one of said plurality of flip flop circuits (41p) serving as a final stage and another (41a) of said plurality of flip flop circuits serving as the first stage, the other or the others (42a to 42c) of said plurality of exclusive-OR gates being supplied with an output bit or output bits from other or others (41a, 41e, 41l) of said plurality of flip flop circuits each located at n-place from said first stage where n is said arbitrary natural number,

and in which each of said terms (X^8, X) of said variable of said one (equation 1) of said polynomials having said term (X^8) with said smaller maximum degree (8) is expressed as X^m where m is another arbitrary natural number, and said plurality of multiplexers (43a/43b) are respectively provided in association with certain flip flop circuits (41a, 41h) selected from said plurality of flip flop circuits each located at m-place from one (41a) of said plurality of flip flop circuits serving as a first stage where m is said another arbitrary natural number.

9. The code generator as set forth in claim 8, in which said one (42d) of said plurality of exclusive-OR gates has input nodes connected to an input terminal (48) supplied with said digital signal (Din) and an output node of one (43b) of said plurality of multiplexers, and said one (43b) of said plurality of multiplexers has input nodes respectively connected to certain flip flop circuits (41h, 41p) selected from said plurality of flip flop circuits and serving as final stages of said plurality of data paths, said output node of said one (43b) of said plurality of multiplexers selectively supplying said cyclic redundancy check codes (CRC8, CRC16) to an output terminal (45),

each of other or others (42a to 42c) of said plurality of exclusive-OR gates has input nodes respectively connected to an output node of the flip flop circuit (41a, 41e, 41l) located at said n-place and an output node of said one of said plurality of exclusive-OR gates (42d) and an output node connected to an input node of a flip flop circuit (41b, 41f, 41m) located at (n+1) place,

each of other or others (43a) of said plurality of multiplexers associated with the flip flop circuit (41a) located at said m-place equal to said n-place having a first input node connected to an output node of said flip flop circuit (41a) located at said m-place, a second input node connected to an output node of the exclusive-OR gate (42a) associated with said flip flop circuit (41a) located at said n-place and an output node connected to an input node of the flip flop circuit (41b) located at (m+1) place.

10. The code generator as set forth in claim 8, in which said one (42d) of said plurality of exclusive-OR gates has input nodes connected to an input terminal (48) supplied with said digital signal (Din) and an output node of one of (43b) said plurality of multiplexers, and said one of said plurality of multiplexers (43b) has input nodes respectively connected to certain flip flop circuits (41h, 41p) selected from said plurality of flip flop circuits and serving as final stages of said plurality of data paths, said output node of said one of said plurality of multiplexers (43b) selectively supplying said cyclic redundancy check codes (CRC8, CRC16) to an output terminal (45),

each of other or others (42a to 42c) of said plurality of exclusive-OR gates has a first input node connected to an output node of the flip flop circuit (41a, 41e, 41l) located at said n-place and an output node connected to an input node of a flip flop circuit (41b, 41f, 41m) located at (n+1) place,

each of other or others (43a) of said plurality of multiplexers associated with the flip flop circuit (41a) located at said m-place equal to said n-place having a first input node connected to an output node of said one (42d) of said plurality of exclusive-OR gate, a second input node connected to a source of predetermined logic level and an output node connected to a second input node of another (42a) of said plurality of exclusive-OR gates located at said n-place equal to said m-place.

BNSDOCID: <EP___0836284A2_I_>

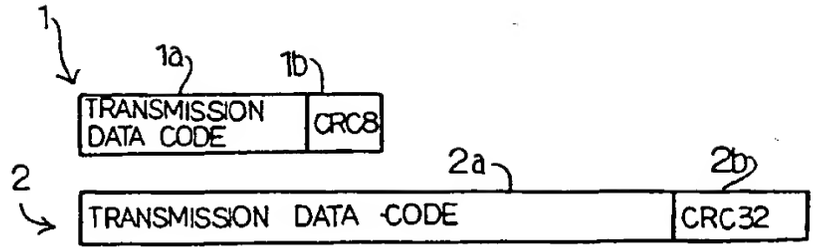


Fig. 1A
PRIOR ART

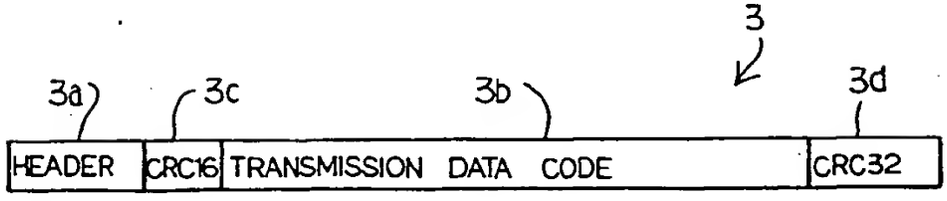


Fig. 1B
PRIOR ART

3NSDOCID: <EP___ 0836284A2_I_>

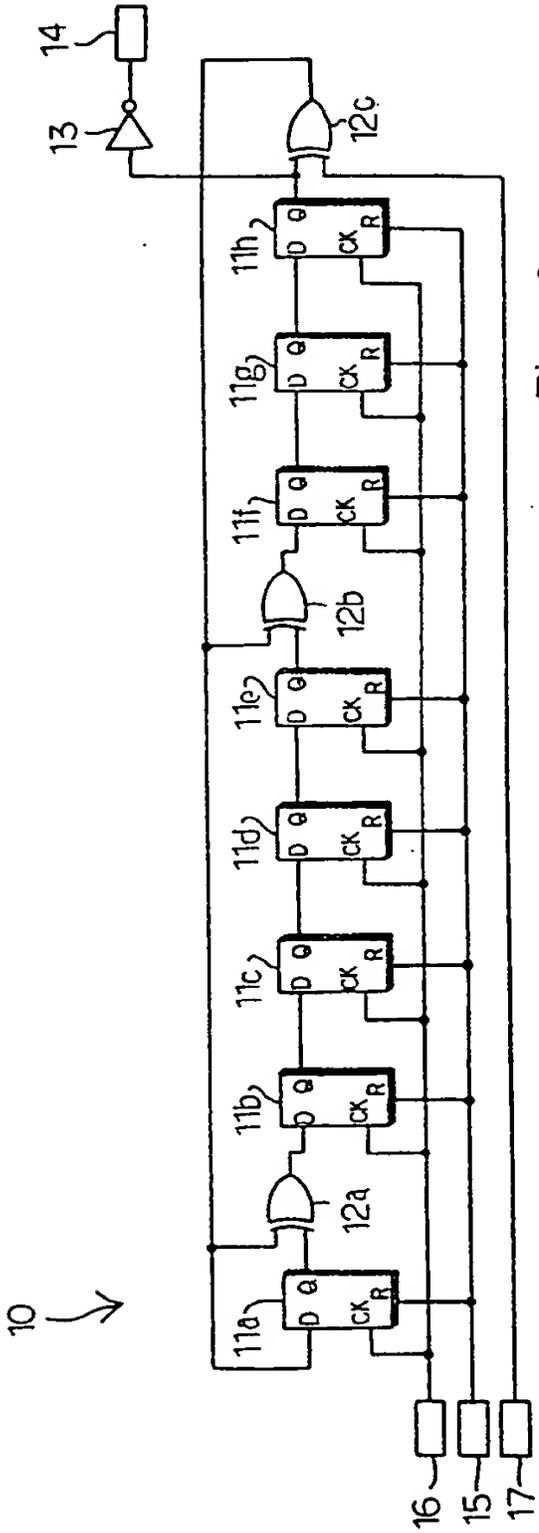


Fig. 2
PRIOR ART

BNSDOCID: <EP___0836284A2_I_>

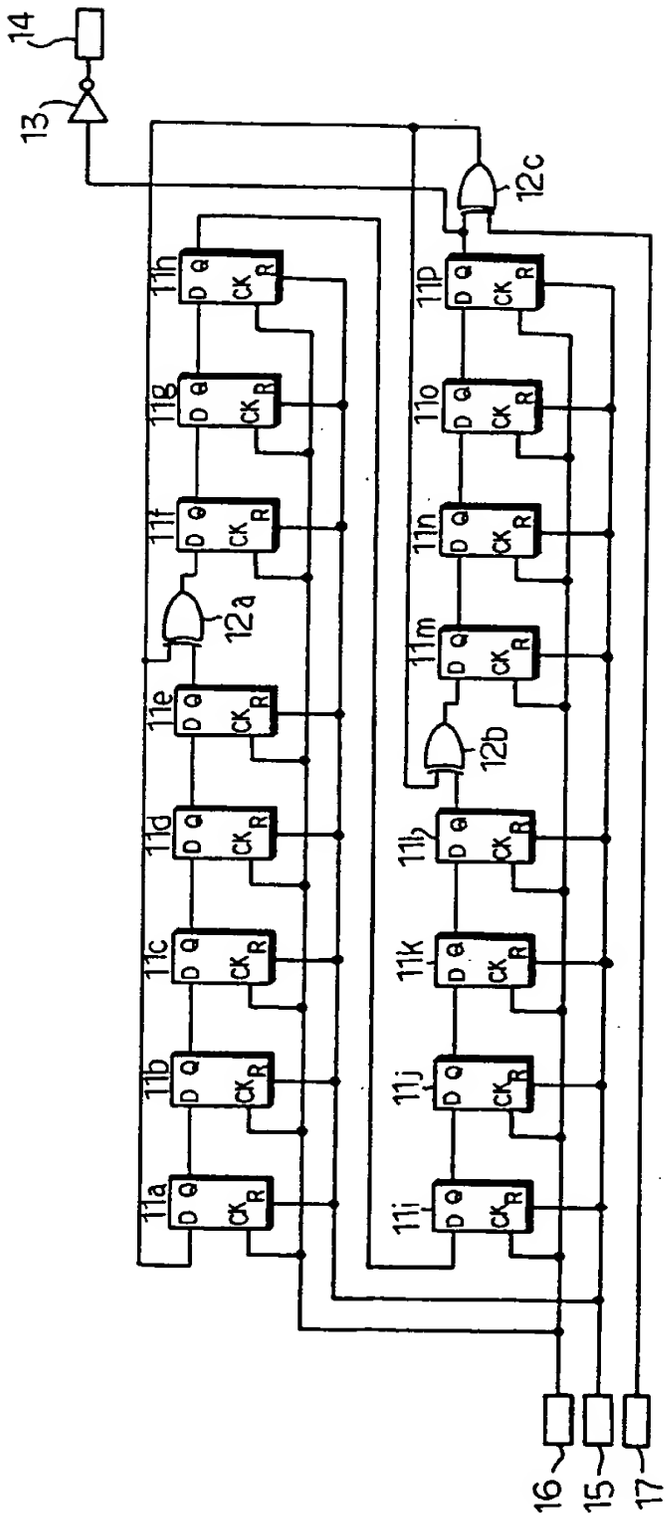


Fig. 3
PRIOR ART

3NSDOCID: <EP_... 0836284A2_I_>

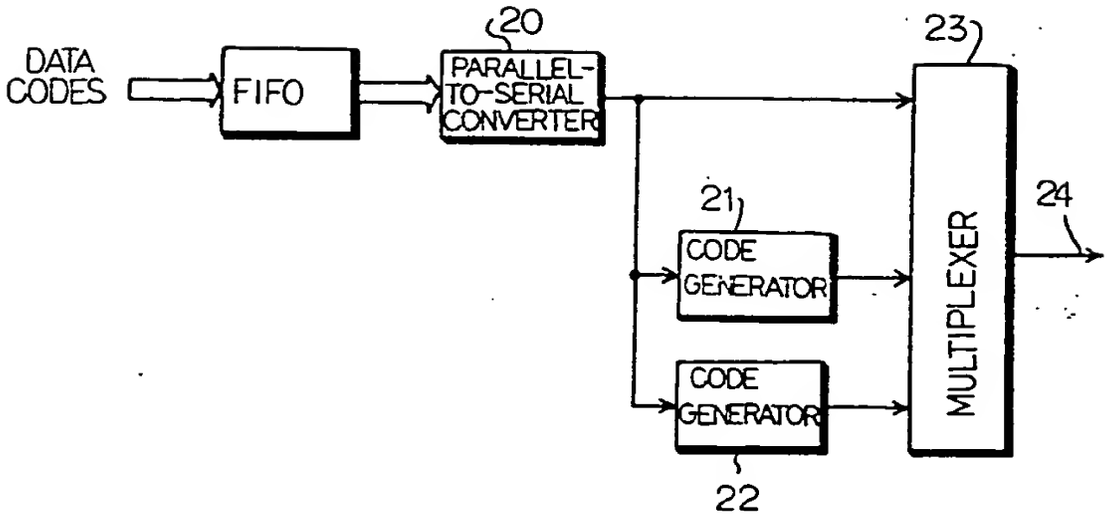


Fig. 4A
PRIOR ART

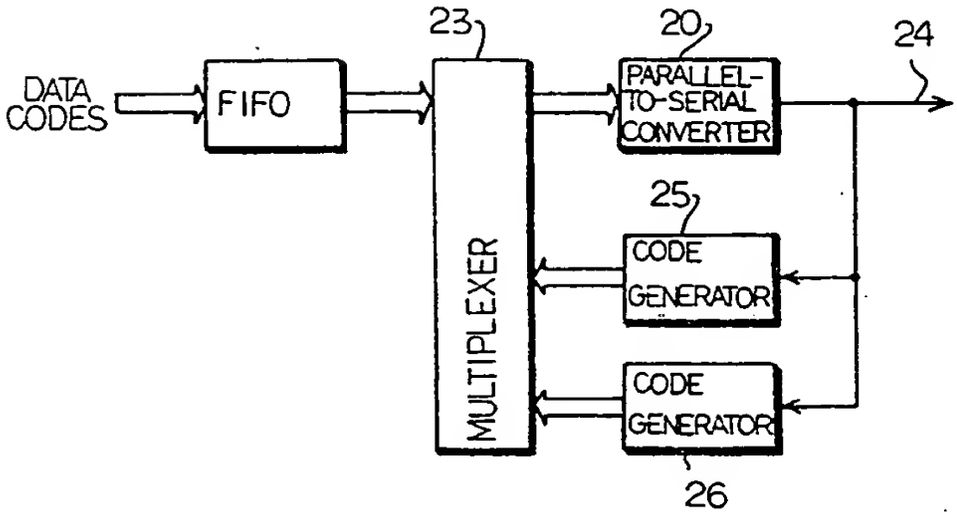


Fig. 4B
PRIOR ART

BNSDOCID: <EP___0836284A2_I_>

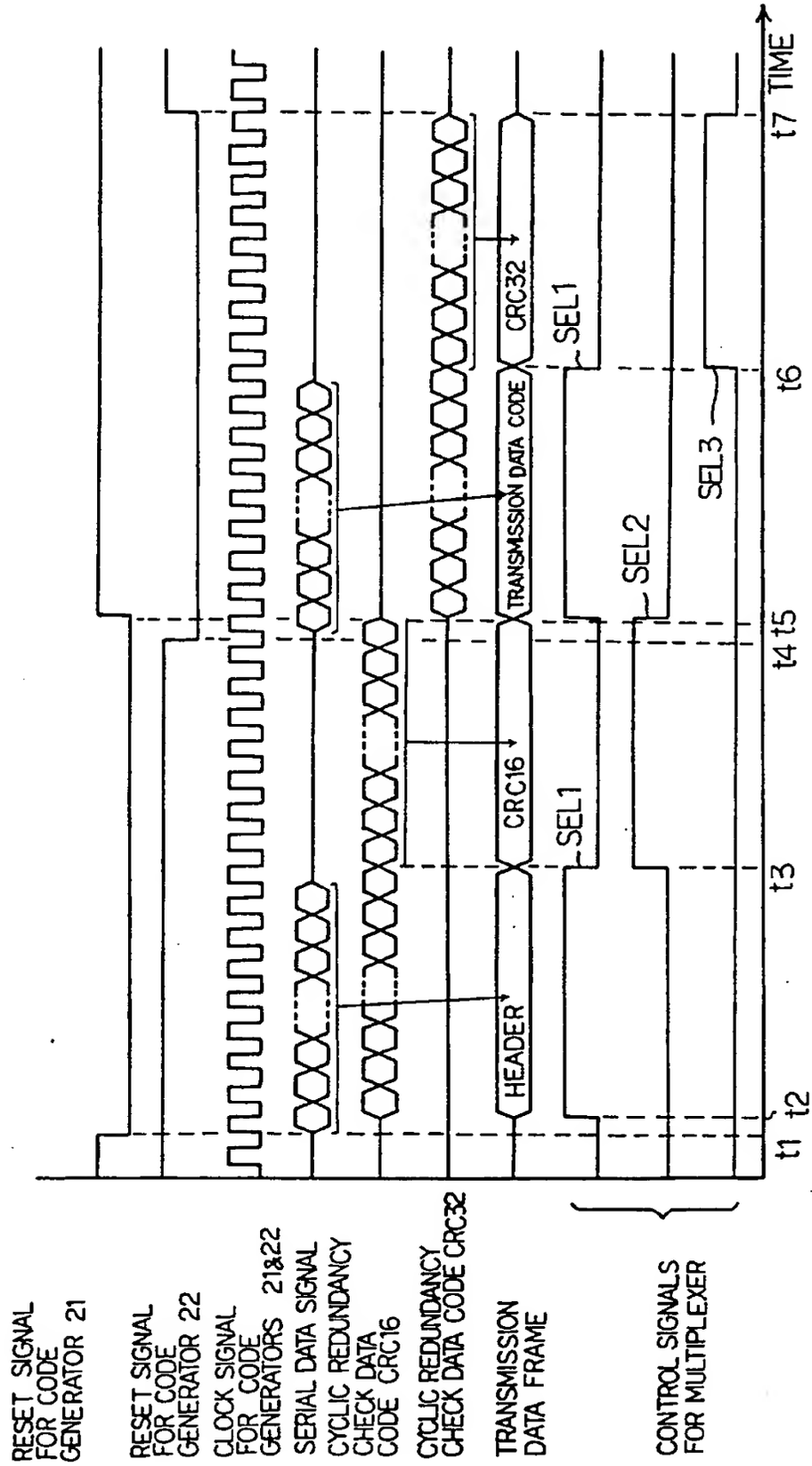


Fig. 5
PRIOR ART

BNSDOCID: <EP_ 0836284A2 I_>

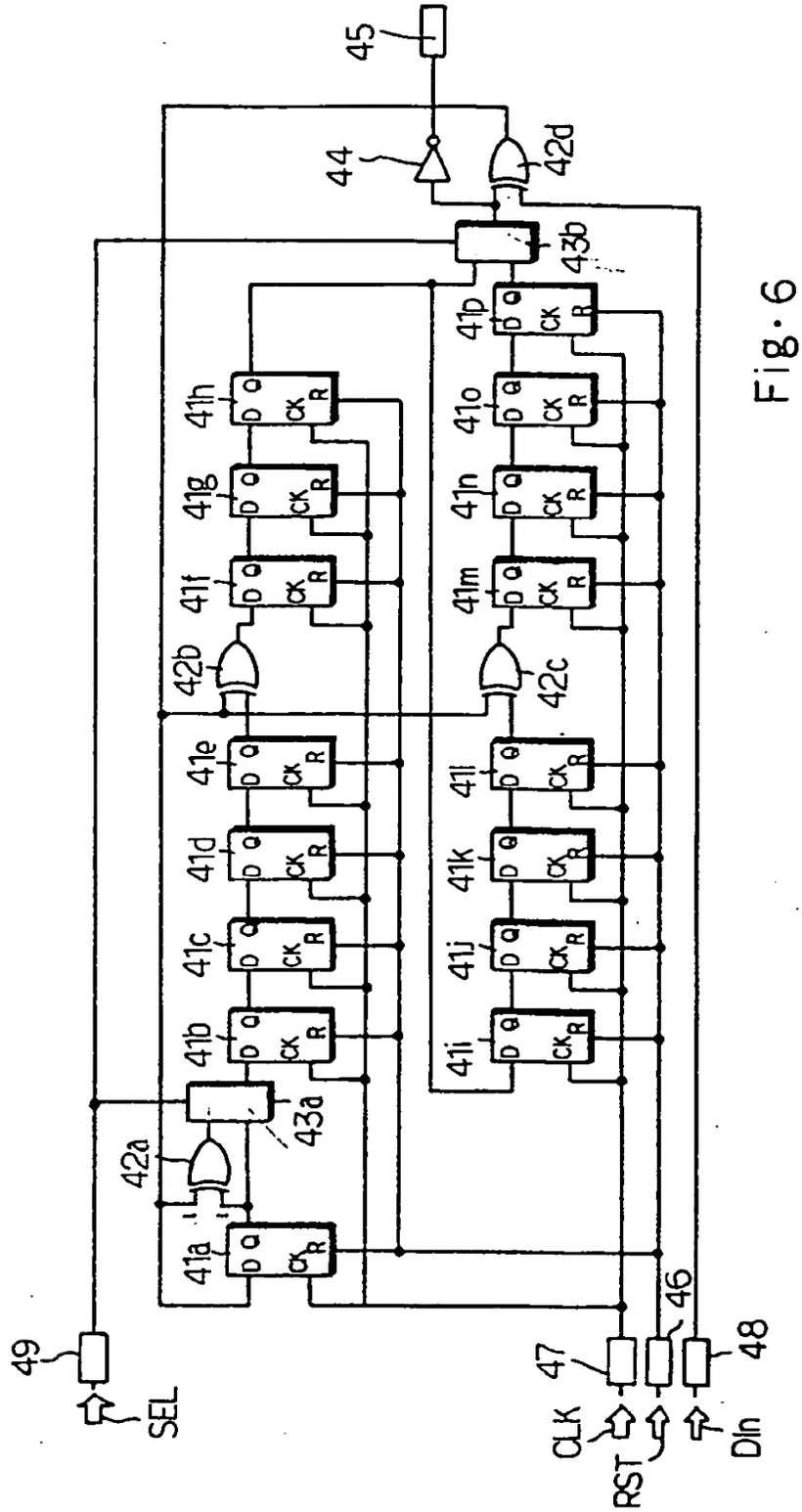
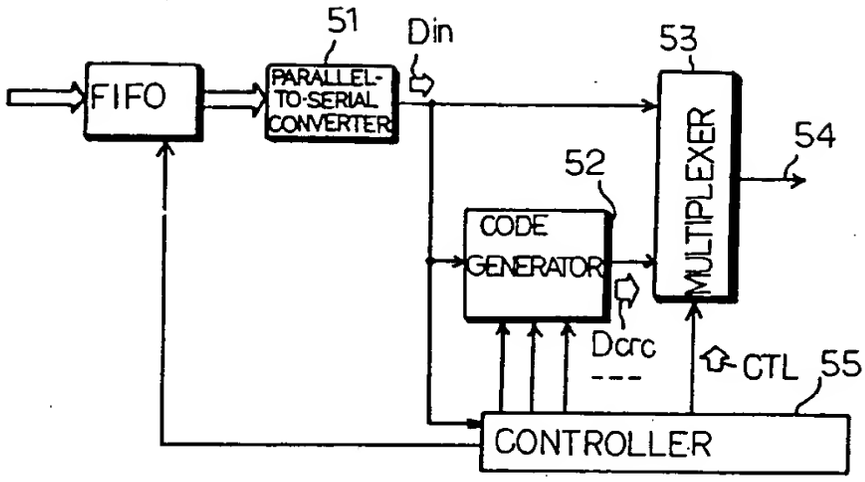


Fig. 6

BNSDOCID: <EP___0836284A2_I_>



Fig·7A

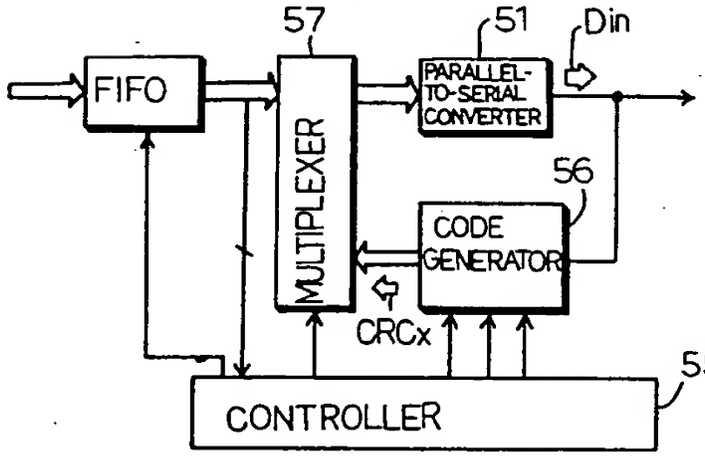


Fig · 7B

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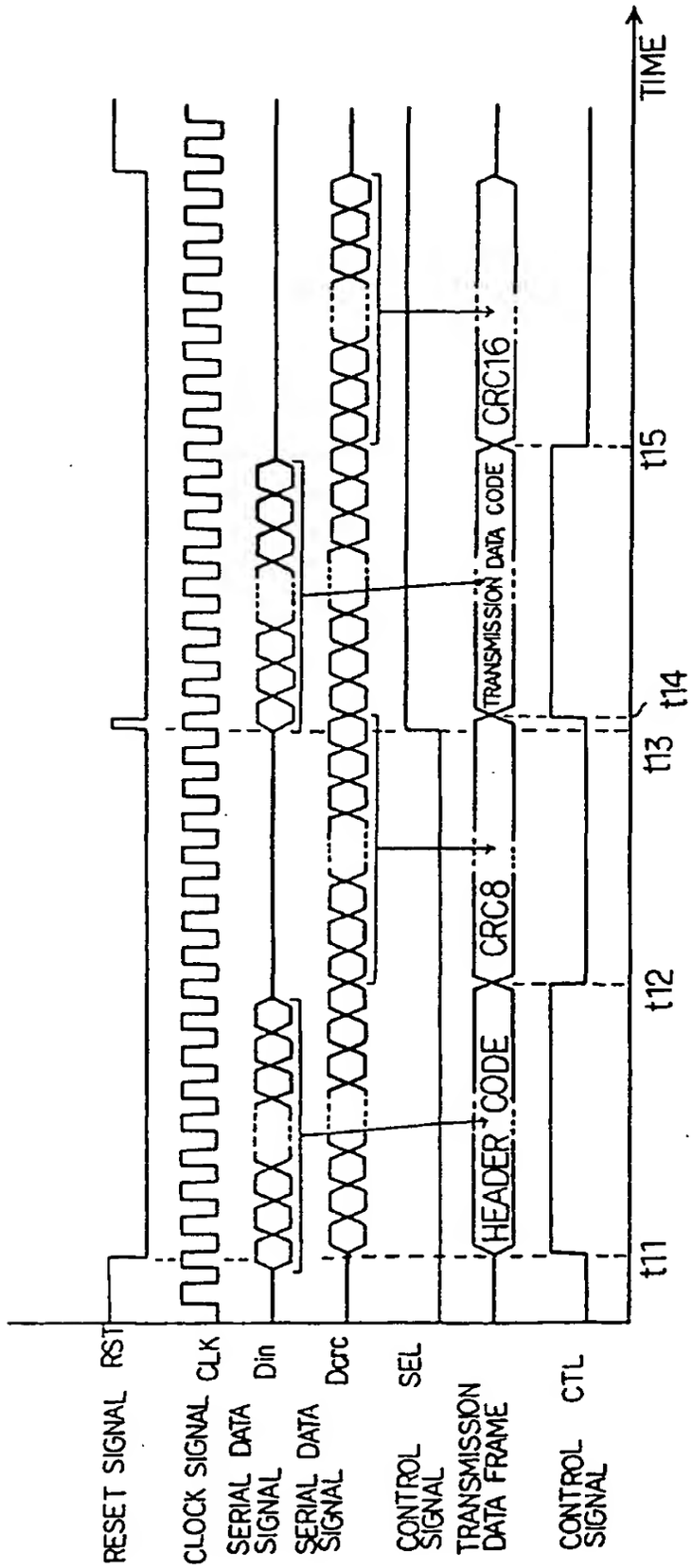

Fig. 8

NSDOCID: <EP___0836284A2_I_>

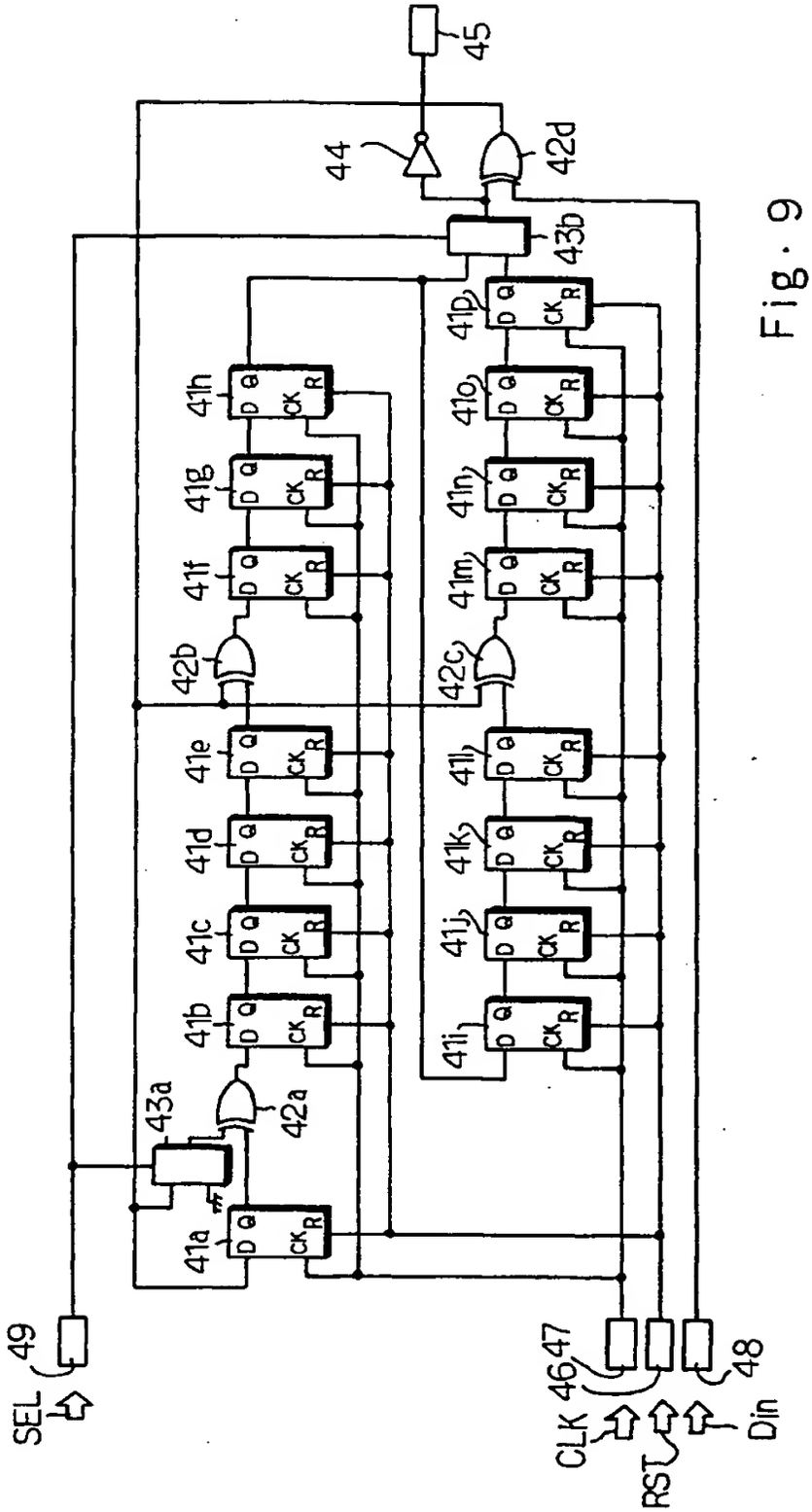

Fig. 9

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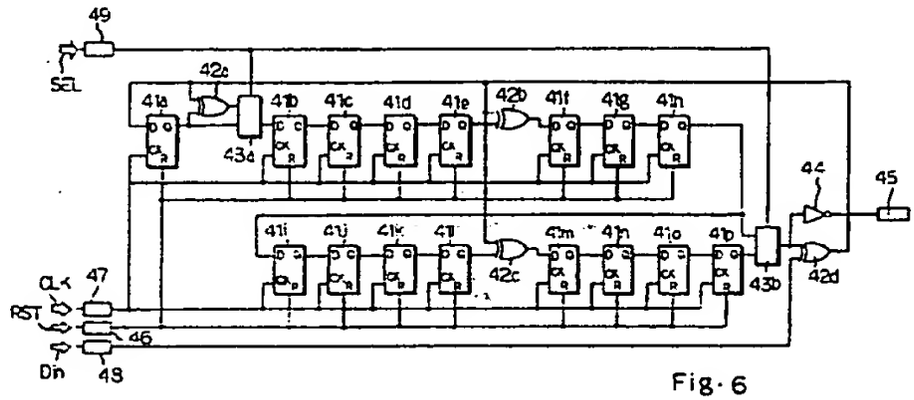
(54) Code generator for selectively producing cyclic redundancy check data codes different in data length

(57) A code generator incorporated in a transmitter has data paths (42d/41a to 41h/42a/43a/42b/43b; 42d/41a to 41p/42a/ 43a/ 42b/42c/43b) different in length for producing one of cyclic redundancy check codes (CRC8, CRC16) different in data length from a digital data signal (Din) supplied thereto, and circuit components of the data path shortest of all are shared with other data paths so that the code generator is fabricated from a small number of circuit components.



Fig·6

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 11 7189

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Y	EP 0 495 642 A (XILINX INC) 22 July 1992 (1992-07-22) * the whole document *	1-10	H03M13/00 H03M13/09 H03M13/35
Y	PATENT ABSTRACTS OF JAPAN vol. 011, no. 083 (F-489), 13 March 1987 (1987-03-13) & JP 61 237521 A (MITSUBISHI ELECTRIC CORP), 22 October 1986 (1986-10-22) * abstract *	1-10	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 December 2000	Devergranne, C

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